Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) A method of fabricating a NAND-type flash memory device, comprising:

forming a plurality of isolation layers running parallel with each other at predetermined regions of a semiconductor substrate;

forming a string selection line pattern~~, a plurality of word line patterns~~ and a ground selection line pattern crossing over active regions between the plurality of isolation layers~~ and active regions between the plurality of isolation layers~~, the string selection line pattern and the ground selection line pattern running parallel with each other;

forming a plurality of word line patterns disposed between the string selection line pattern and the ground selection line pattern;

ion-implanting impurities into the active regions among the string selection line pattern, the plurality of word line patterns and the ground selection line pattern, thereby forming drain regions at the active regions adjacent to the string selection line pattern and opposite the ground selection line pattern and concurrently forming source regions at the active regions adjacent to the ground selection line pattern and opposite the string selection line pattern;

forming a first interlayer insulating layer on the entire surface of the substrate including the drain and source regions;

patterning the first interlayer insulating layer to form a slit-type common source line contact hole exposing the source regions and the isolation layers between the source regions; and

forming a common source line filling the common source line contact hole~~;~~

~~wherein a top surface level of the common source line is even with or lower than a top~~

~~surface level of the first interlayer insulating layer.~~ such that the common source line is disposed on the source regions and the isolation layers between the source regions, the common source line running parallel with the ground selection line pattern and being electrically connected to the source regions.

2. (Original) The method of Claim 1, wherein forming the first interlayer insulating layer is preceded by the step of forming an etch stop layer having an etch selectivity with respect to the first interlayer insulating layer on the entire surface of the substrate including the source and drain regions.

3. (Original) The method of Claim 2, wherein forming the common source line contact hole comprises:

patterning the first interlayer insulating layer to expose the etch stop layer on the source regions and the isolation layers between the source regions; and

etching the exposed etch stop layer to expose the source regions and the isolation layers between the source regions.

4. (Original) The method of Claim 1, wherein forming the common source line comprises the steps of:

forming a conductive layer filling the common source line contact hole on the entire surface of the substrate including the common source line contact hole; and

planarizing the conductive layer until the first interlayer insulating layer is exposed.

5. (Original) The method of Claim 1, wherein forming the common source line comprises:

forming a doped polysilicon layer filling the common source line contact hole on the entire surface of the substrate including the common source line contact hole;

planarizing the doped polysilicon layer until the first interlayer insulating layer is exposed, thereby forming a common source line contact plug in the common source line contact hole; and

selectively forming a metal silicide layer on the surface of the common source line contact plug.

6. (Original) The method of Claim 1, wherein forming the common source line is followed by the steps of:

forming a second interlayer insulating layer on the entire surface of the substrate including the common source line;

sequentially patterning the second interlayer insulating layer and the first interlayer insulating layer to form bit line contact holes exposing the respective drain regions;

forming bit line contact plugs in the respective bit line contact holes;

forming a metal layer on the entire surface of the substrate including the bit line contact plugs; and

patterning the metal layer to form a plurality of bit lines electrically connected to the respective bit line contact plugs, the plurality of bit lines crossing over the plurality of word line patterns and the common source line.

7. (Currently Amended) A method of fabricating a NAND-type flash memory device, comprising:

forming a plurality of isolation layers running parallel with each other at predetermined regions of a semiconductor substrate;

forming a string selection line pattern~~, a plurality of word line patterns~~ and a ground selection line pattern crossing over active regions between the plurality of isolation layers ~~and active regions between the plurality of isolation layers~~, the string selection line pattern and the ground selection line pattern running parallel with each other;

forming a plurality of word line patterns disposed between the string selection line pattern and the ground selection line pattern;

ion-implanting impurities into the active regions among the string selection line pattern, the plurality of word line patterns and the ground selection line pattern, thereby forming drain regions at the active regions adjacent to the string selection line pattern and opposite the ground selection line pattern and concurrently forming source regions at the active regions adjacent to the ground selection line pattern and opposite the string selection line pattern;

forming a first interlayer insulating layer on the entire surface of the substrate including the drain and source regions;

patterning the first interlayer insulating layer, thereby forming a slit-type common source line contact hole exposing the source regions and the isolation layers between the source regions and concurrently forming a plurality of drain contact holes exposing the respective drain regions; and

forming a common source line filling the common source line contact hole and a plurality of drain contact plugs filling the respective drain contact holes, such that the common source line is disposed on the source regions and the isolation layers between the source regions, the common source line running parallel with the ground selection line pattern and being electrically connected to the source regions,

wherein a top surface level of the common source line is even with or lower than a top surface level of the first interlayer insulating layer.

8. (Original) The method of Claim 7, wherein forming the first interlayer insulating layer is preceded by the step of forming an etch stop layer having an etch selectivity with respect to the first interlayer insulating layer on the entire surface of the substrate including the source and drain regions.

9. (Original) The method of Claim 8, wherein forming the common source line contact hole and the plurality of drain contact holes comprises:

patterning the first interlayer insulating layer to expose the etch stop layer on the drain regions, the source regions and the isolation layers between the source regions; and

etching the exposed etch stop layer to expose the drain regions, the source regions and the isolation layers between the source regions.

10. (Original) The method of Claim 7, wherein forming the common source line and the drain contact plugs comprises:

forming a conductive layer filling the common source line contact hole and the drain contact holes on the entire surface of the substrate including the common source line contact hole and the drain contact holes; and

planarizing the conductive layer until the first interlayer insulating layer is exposed.

11. (Original) The method of Claim 7, wherein forming the common source line and the drain contact plugs comprises:

forming a doped polysilicon layer filling the common source line contact hole and the drain contact holes on the entire surface of the substrate including the common source line contact hole and the drain contact holes;

planarizing the doped polysilicon layer until the first interlayer insulating layer is exposed, thereby forming a first polysilicon pattern and second polysilicon patterns in the common source line contact hole and the respective drain contact holes, respectively; and selectively forming a metal silicide layer on the first and second polysilicon patterns.

12. (Original) The method of Claim 7, wherein forming the common source line and the drain contact plugs is followed by:

forming a second interlayer insulating layer on the entire surface of the substrate including the common source line and the drain contact plugs;

patterning the second interlayer insulating layer to form bit line contact holes exposing the respective drain contact plugs and a metal contact hole exposing a portion of the common source line;

forming a metal layer on the entire surface of the substrate including the bit line contact holes and the metal contact hole; and

patterning the metal layer to form a plurality of bit lines electrically connected to the respective drain contact plugs and a metal interconnection electrically connected to the common source line, the plurality of bit lines and the metal line crossing over the plurality of word line patterns and the common source line.